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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,710	10/29/2003	Lung T. Tran	10017427-1	5581

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,710	TRAN ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-12,15 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-12,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on 07/20/2005 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent 6,541,792 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Specification

2. Claim 15 is objected to because of the following informalities: Claim 15 recites: "the first tunnel junction" which lacks an antecedent basis. It is clear from the description that the barrier layer (124) and the bottom conductor (106 or 122) constitute the first tunnel junction (103). Therefore, for examination purposes, claim 15 is interpreted as follows:

A memory element comprising:

an anti-fuse comprising a bottom conductor, a top conductor, and a barrier layer of non-uniform thickness therebetween, the barrier layer and the bottom conductor constituting a first tunnel junction; and

an isolator element in series with the first tunnel junction;

wherein the barrier layer has a dielectric breakdown voltage of between 2 and 3 volts.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 9-10** are rejected under 35 U.S.C. 102(e) as being anticipated by Van Brocklin et al. U.S. Patent 6,870,751 (the '751 reference).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Referring to **claims 9-10**, the '751 reference discloses an antifuse tunnel junction for use in a memory element, comprising:

a bottom conductor (106, Fig. 2) comprising an upper surface;

a top conductor (108); and

a barrier layer (storage element 204, column 5, lines 4-10, when used as an antifuse is a tunnel barrier layer, column 3, second paragraph) disposed between the bottom conductor and the top conductor;

wherein the barrier layer (204) of the antifuse tunnel junction comprises a non-uniform surface.

4. **Claims 9-10** are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al. U.S. Patent 6,841,846 (the '846 reference).

Referring to **claims 9-10**, the '846 reference discloses an antifuse tunnel junction for use in a memory element, comprising:

a bottom conductor (14, Fig. 1) comprising an upper surface;

a top conductor (22); and

a barrier layer (16, column 2, lines 44-53) disposed between the bottom conductor and the top conductor;

wherein the barrier layer (16) of the antifuse tunnel junction (14/16) comprises a non-uniform surface (note that although the '846 reference does not explicitly call antifuse junction (14/16) an antifuse tunnel junction, antifuse junction (14/16) is an antifuse tunnel junction, because of its appropriate thickness (column 3, lines 1-15, and consults the '751 reference, cited above, column 3, lines 12-25, which teaches that tunneling could happen at thickness greater than 50 angstroms, and see Gosain et al. U.S. Patent 6,285,055, column 13, lines 55-62, which teaches that tunneling phenomenon happens even at thickness of hundreds of angstroms (tens of nm))).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claim 15** is rejected under 35 U.S.C. §103(a) as being unpatentable over Bracchitta et al. U.S. Patent 6,020,777 (the '777 reference) in view of Cleeves et al. U.S. Patent Application Publication 20030003632 (the '632 reference).

The '777 reference discloses a memory element comprising:

an anti-fuse (capacitive antifuse 10, Fig. 1, column 3, lines 5-59; and see Fifield et al. U.S. Patent Application Publication 20050073023, paragraph [0006], for a clear definition that an antifuse is considered a capacitor) comprising a bottom conductor (no number) , a top conductor (no number), and a barrier layer (no number, also termed capacitor dielectric, barrier dielectric, or tunnel dielectric, by artisans in the art, depending on the materials of the layer), the barrier layer and the bottom conductor constituting a first tunnel junction (column 3, lines 5-59, particularly lines 48-50); and

an isolator element (11) in series with the first tunnel junction;

wherein the barrier layer has a dielectric breakdown voltage of about 2 volts (column 3, lines 18-21), meeting the claimed range of between 2 and 3 volts.

However, the '777 reference fails to disclose that the barrier layer has a non-uniform thickness.

The '632 reference, in also disclosing a memory structure including a memory element, teaches in paragraph [0006] that it has been known for many years that electrical fields can be enhanced at sharp corners, rough surfaces and the like, and further teaches that such enhanced electric fields are used to assist in transferring electrical charge through tunneling and avalanche injection.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '777 reference's barrier layer such that it has a non-uniform

thickness as claimed. One would have been motivated to make such a change in view of the teachings in the '632 reference that such a layer with a non-uniform thickness, or rough surfaces, assist in transferring electrical charge through tunneling.

6. **Claims 11-12 and 15-16** are rejected under 35 U.S.C. §103(a) as being unpatentable over Fifield et al. U.S. Patent Application Publication 20050073023 (the '023 reference) in view of Cleeves et al. U.S. Patent Application Publication 20030003632 (the '632 reference).

Referring to **claims 10, 12 and 15**, the '023 reference discloses a memory element including an antifuse tunnel junction having a tunnel barrier layer as claimed but fails to teach that the tunnel barrier layer of the antifuse tunnel junction has a non-uniform thickness and further fails to teach that the barrier layer has a dielectric breakdown voltage of between 2 and 3 volts as claimed.

Specifically, the '023 reference discloses an antifuse tunnel junction for use in a memory element, comprising:

a bottom conductor (136A, Fig. 2) comprising an upper surface;

a top conductor (132A); and

a barrier layer (140A, paragraph [0026]) disposed between the bottom conductor and the top conductor;

wherein the barrier layer has a dielectric breakdown voltage of about 3.5 volts (in one embodiment, paragraph [0041]), instead of the claimed range of between 2 and 3 volts.

And a memory element comprising:

an anti-fuse (128) comprising a bottom conductor (136A, Fig. 2), a top conductor (132A), and a barrier layer (140A), the barrier layer and the bottom conductor constituting a first tunnel junction; and

an isolator element (124) in series with the first tunnel junction;

wherein the barrier layer has a dielectric breakdown voltage of about 3.5 volts (in one embodiment, paragraph [0041]), instead of the claimed range of between 2 and 3 volts.

However, the '023 reference fails to disclose that the barrier layer of the antifuse tunnel junction has a non-uniform thickness.

The '632 reference, in also disclosing a memory structure including a memory element, teaches in paragraph [0006] that it has been known for many years that electrical fields can be enhanced at sharp corners, rough surfaces and the like, and further teaches that such enhanced electric fields are used to assist in transferring electrical charge through tunneling and avalanche injection.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '023 reference's barrier layer such that it has a non-uniform thickness as claimed. One would have been motivated to make such a change in view of the teachings in the '632 reference that such a layer with a non-uniform thickness, or rough surfaces, assist in transferring electrical charge through tunneling.

As noted above, the mentioned teachings teach that the barrier layer has a dielectric breakdown voltage of about 3.5 volts (in one embodiment, paragraph [0041], the '023 reference), instead of the claimed range of between 2 and 3 volts. However, the different in the size of the

breakdown voltages is deemed to be obvious because a change in size is recognized as being within the level of ordinary skill in the art (MPEP 2144.04 [R-1], section IV).

Referring to **claim 11**, the '023 reference further discloses that the thickness, or average thickness as modified in view of the '632 reference to have a non-uniform thickness, is about 17 angstroms (paragraph [0041], 17 Å), meeting the claimed range of between 10 and 30 angstroms.

Referring to **claim 16**, the '023 reference further discloses that the isolator element (124) is a second tunnel junction (paragraph [0026]), meeting the limitation of the claimed Markush group of a second tunnel junction, a magnetic tunnel junction, a diode and a resistor.

7. **Claims 1-2 and 4-8** are rejected under 35 U.S.C. §103(a) as being unpatentable over Fifield et al. U.S. Patent Application Publication 20050073023 (the '023 reference) in view of Cleeves et al. U.S. Patent Application Publication 20030003632 (the '632 reference), further in view of Yuan et al. U.S. Patent 5,965,913 (the '913 reference) or in view of Harari U.S. Patent Application Publication 20030218920 (the '920 reference), and further in view of knowledge in the art.

Referring to **claims 1 and 4-7**, the '023 reference discloses a memory device including at least one memory element having an antifuse tunnel junction including a tunnel barrier layer and a bottom conductor as claimed but fails to teach that the bottom conductor comprises a non-uniform upper surface and also fails to teach that the memory device is arranged in a cross-point arrangement including a plurality of word lines and a plurality of bit lines and arranged such that the at least one memory element further comprises one of the memory elements formed at each cross point as claimed.

Specifically, the '023 reference discloses a resistive array memory device, comprising:

at least one memory element (128, Fig. 2), the memory element comprising an antifuse tunnel junction (paragraph [0026]), having a bottom conductor (136A, Fig. 2), a top conductor (132A), and a barrier layer (140A, paragraph [0026]) adjacent the bottom conductor;

However, the '023 reference fails to disclose that the bottom conductor comprises a non-uniform upper surface.

The '632 reference, in also disclosing a memory structure including a memory element, teaches in paragraph [0006] that it has been known for many years that electrical fields can be enhanced at sharp corners, rough surfaces and the like, and further teaches that such enhanced electric fields are used to assist in transferring electrical charge through tunneling and avalanche injection. The rough surfaces, as detailed above, would logically be formed as a result of dielectric barrier layers having non-uniform thickness. In other words, from the teaching of the '632 reference, it would have been obvious only to conclude that the roughness of the surfaces are the roughness of the tunnel barrier layers, and not so obvious as to be the roughness of the underlying upper surface of the underlying conductive layer that forms an interface with the overlying tunnel barrier layer that together form the tunnel barrier junction that causes the tunneling phenomenon.

The '913 reference and the '920 reference each, in also disclosing a memory structure including a memory element, teaches that the roughness, also for the purpose of enhancing electrical fields in assisting in transferring electrical charge through tunneling, could come from the underlying upper surface of the underlying conductive layer that forms an interface with the overlying tunnel barrier layer that together form the tunnel barrier junction that causes the

tunneling phenomenon (the '913 reference, column 15, first full paragraph; the '920 reference, paragraph [0245]), which underlying upper surface of the underlying conductive layer that forms an interface with the overlying tunnel barrier layer that together form the tunnel barrier junction that causes the tunneling phenomenon could be called an upper surface of a bottom conductor for short. In other words, each of the references teaches a conductor that has a non-uniform surface, and, as applied in the instant particular orientation of directions, a bottom conductor that has a non-uniform upper surface.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '023 reference's bottom conductor such that it comprises a non-uniform upper surface as claimed. One would have been motivated to make such a change in view of the teachings in the '632 reference, the '913 reference and the '920 reference, that such a layer with a non-uniform upper surface, or rough surfaces, or surfaces with asperities, assist in transferring electrical charge through tunneling.

As noted above, the mentioned teachings teach that the barrier layer has a dielectric breakdown voltage of about 3.5 volts (in one embodiment, paragraph [0041], the '023 reference), instead of the claimed range of between 2 and 3 volts. However, the different in the size of the breakdown voltages is deemed to be obvious because a change in size is recognized as being within the level of ordinary skill in the art (MPEP 2144.04 [R-1], section IV), and as noted above, the '023 reference further discloses that the isolator element (124) is a second tunnel junction (paragraph [0026]), meeting the limitation of the claimed Markush group of a second tunnel junction, a magnetic tunnel junction, a diode and a resistor.

And, as detailed above, the mentioned teaching fails to teach that the memory element is arranged in a cross-point arrangement including a plurality of word lines and a plurality of bit lines and arranged such that the at least one memory element further comprises one of the memory elements formed at each cross point as claimed.

However, at the time the invention was made, resistive memory devices including at least one memory element were typically arranged in a cross-point arrangement including a plurality of word lines and a plurality of bit lines, to access the at least one memory element, and arranged such that the at least one memory element further comprises one of the memory elements formed at each cross point. For such an arrangement, consult U.S. Patent 6,005,800 to Koch et al., Figs. 1. Since such an arrangement was one of arrangements known to a person of ordinary skill in the art at the time the invention was made, such an arrangement would have been obvious.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
September 09, 2005